DETERMINATION OF DRAIN CURRENT SATURATION ATTENUATION FOR SHORT CHANNEL MOSFETS

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Abstract
Carrier saturation velocity is one of the most important device parameters in determining the performance of the enhancement MOSFETs. Therefore, the saturation of drain current $I_{dsat}$ in short channel MOS devices is caused by the carrier velocity saturation. For the linear region device characteristics, the dependence of inversion layer mobility on the gate field is important and it has been extensively studied. For the saturation region characteristics $I_{dsat}$ of short channel MOSFETs, the scattering limited carriers velocity $v_{sat}$ is of a dominant importance. As a result, the non ohmic characteristic of devices is severely reduced. In this work, a plausible explanation is provided for the reduction of drain current saturation $I_{dsat}$.

Keywords: MOSFETs; Velocity Saturation; CLM; DIBL; Pinch off.

1. Introduction
In short channel MOSFETs, drain current characteristic in saturation region varies weakly against drain voltage in non-ohmic regime. Therefore, it implies a zero dynamic conductance $G_d(V_d)$. It has been difficult to model $I_{dsat}$ correctly, major short channel effects and hot carrier effect, such as channel length modulation (CLM) [1], drain-induced-barrier-lowering DIBL [2-5] and substrate current induced output resistance reduction [6-7] are all influencing $I_{dsat}$ determination. Because MOSFET model in the linear region is fairly well understood, we will concentrate only on the saturation region in this paper. To achieve high accuracy and scalability, $I_{dsat}$ model must be analytically equal to long channel device characteristic $I_d(V_d)$. This analytical model includes a reduction term which is due to velocity saturation phenomena.

2. Model
The operation mode in non-ohmic regime consisted in applying important voltage on the drain in addition to the applied gate voltage. The inversion layer, which is evenly distributed in the channel, should be more pinched close to the drain. At the voltage value $V_d$ equals $V_{dsat}$ the charge at the drain level becomes very weak (pinch off). For the drain voltage $V_d$ exceeding $V_{dsat}$ this charge doesn't vary practically. The transistor is saturated on the length $\Delta L$ [8]. In the case of short channel MOSFET, the drain current is limited by velocity saturation, and its value depends on both the saturation voltage value and the transistor velocity saturation. Therefore, the drain current expression is related to inversion charge $Q_i$ and carrier drift velocity by

$$I = WQ_i v,$$

where $W$ is the channel width and $v$ is the carriers drift velocity. For short channel devices, the inversion charge $Q_i$ in strong inversion, is controlled by both gate and drain voltage respectively, such as

$$Q_i = C_{ox}(V_g - V_t - V(y)),$$

where $C_{ox}$ is the oxide capacitance per unit area, $V_t$ is the threshold voltage and $V(y)$ is the voltage along the channel at $y$ space. Under stationary transport conditions the electron drift velocity can be written as

$$v = \mu_e E_0,$$

where $\mu_e$ is the mobility, $E_0$ is the electrical field which is obeying to gradual channel approximation as follows

$$E_0 = \frac{dV}{dy}.$$

Including Eqs. (2) and (3) into drain current expression, we obtain

$$I = \mu_e W C_{ox}(V_g - V_t - V(y))E_0.$$

Moreover, the drift velocity reduction for short channel device, is written as

$$v = \mu E',$$

where $E'$ is the electrical field which is given by Sodini's law [9] as follows

$$E' = \frac{E_0}{1 + \frac{E_0}{E_c}},$$
where $E_c$ is the critical field. Therefore, the drain current expression is re-arranged as

$$I = \mu_e W C_a (V_g - V_t - V_f(y)) \left( \frac{dV}{dy} \right) \left( 1 + \frac{dV}{dy} / E_c \right) . \quad (8)$$

By integrating equation (8) between drain and source, one obtains the drain current such as

$$I_d = \mu_e \frac{W}{L} C_a (V_g - V_t - V_d/2) V_d \left( 1 + \frac{V_d}{E_c L} \right) . \quad (9)$$

Eq. (9) is re-arranged and drain current saturation becomes

$$I_{sat} = \mu_e \frac{W}{2L} C_a (V_g - V_t)^2 \left( 1 + \theta_c (V_g - V_t) \right) , \quad (10)$$

which can be also written as

$$I_{sat} = I_{ext} \left( 1 + \theta_c (V_g - V_t) \right) , \quad (11)$$

where $\theta_c$ is defined as a reduction coefficient and it is related to the critical field $E_c$ and channel length $L$ by: $(\theta_c = 1/E_c L)$. $I_{sat}$ and $I_{ext}$ are drain current saturations for short and long channel devices, respectively.

**3. Results and discussion**

As MOSFET channel lengths are scaled to short channel dimensions with a corresponding reduction of power supply voltage, the device operates more and more in the velocity saturated mode, which severely limits current derivability. For example, in $0.25 \mu m$ and $0.8 \mu m$ NMOS $I_d(V_d)$ curves shown in Figs. 1 and 2 respectively, the drain current saturates at drain voltage much less than the long channel saturation voltage, $V_{sat} = V_g - V_t$. The first assumption Eq. (3) is based on the gradual channel approximation, which asserts that the lateral field is much smaller than the transverse field in the channel of MOSFET. This assumption is clearly violated in short channel MOSFET where velocity saturation reduction Eq. (6) is of interest, as it has been manifested in drain current model Eq. (8). In order to evaluate the saturation current reduction we have defined a new parameter called $\theta_c$, which is a reduction coefficient of drain current saturation Eq. (10). For long channel devices $\theta_c$ is null and for decreasing channel lengths $L$, $\theta_c$ increases, as described in Figs. 3 and 4. Moreover, the parameter $\theta_c$ can be easily extracted using optimization techniques to get the best fit between theoretical expression Eq. (10) and $I_{sat}(V_d)$ experimental data. The drain current saturation for the long channel $I-V$ curve is reduced by a factor 2.43 as shown in Fig. 4 for $L=0.25 \mu m$ and by a factor 1.53 for $L=0.8 \mu m$ as shown in Fig. 3. The extracted values of $\theta_c$ are indicated in the Table 1.

As the channel length scaled down, the effect of coefficient $\theta_c$ becomes more and more pronounced, for $L = 0.25 \mu m$, $\theta_c = 0.712 V^{-1}$ and for $L = 0.8 \mu m$, $\theta_c = 0.128 V^{-1}$ as showing in Figs. 1 and 2, respectively.

<table>
<thead>
<tr>
<th>N Conventional MOSFETs</th>
<th>Vg(V)</th>
<th>Vt(V)</th>
<th>$\theta_c(V^{-1})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L=9.5/0.25</td>
<td>2.5</td>
<td>0.5</td>
<td>0.712</td>
</tr>
<tr>
<td>W/L=9.5/0.8</td>
<td>4.95</td>
<td>0.8</td>
<td>0.128</td>
</tr>
</tbody>
</table>

**Table 1 : Reduction coefficient values for two different channel lengths.**

![Figure 1: Drain current $I_d$ versus drain voltage $V_d$ for (W/L = 9.5/0.25) NMOS device.](image1.png)

![Figure 2: Drain current $I_d$ versus drain voltage $V_d$ for (W/L = 9.5/0.8) NMOS device.](image2.png)
4. Conclusion

The attenuation drain current in short channel MOSFETs has been characterized using a simple model. It is found that, drain current saturation has been reduced by a meaningful attenuation factor, namely $\theta_c$. Indeed, $\theta_c$ is defined as a reduction coefficient of drain current saturation $I_{dsat}$.

Results of this study also indicate that drain current saturates at drain voltage less than that of long channel saturation voltage, $V_{dsat} = V_g - V_t$. These results are useful for developing and testing theoretical drain current models, and are of practical importance in estimating the ultimate speed performance of short channel devices.

References